EXHIBIT B

Substitute Preliminary Amendment to correct the Preliminary Amendment Filed Sept 25, 2000 for compliance with 37 CFR 1.52(a).

Atty. Docket No. RA001C11
Application No. 09/669,295

B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Case No. **RA001C11**)

In the Application of:	)	
	)	
FARMWALD ET AL.	)	**Group**
	)	**Art Unit:** 2781
Serial No: Continuation of 09/510,213	)	
	)	**Before**
Filed: FEBRUARY 22, 2000	)	**Examiner:** G. Auve'
	)	
Title: METHOD OF OPERATING A MEMORY HAVING A VARIABLE DATA OUTPUT LENGTH	)	

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE ABSTRACT:

Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

IN THE TITLE:

Please delete the title and substitute "METHOD OF OPERATION OF A MEMORY CONTROLLER".

IN THE SPECIFICATION:

On page 1, line 8, insert --This application is a continuation of Application No. 09/510,213, filed on February 22, 2000 (still pending), which is a continuation of Application No. 09/252,998, filed on February 19, 1999 (now U.S. Patent 6,032,214), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No. 08/762,139, filed on December 9, 1996 (now U.S. Patent 5,809,263); which is a continuation of Application No. 08/607,780, filed February 27, 1996 (now abandoned); which is a continuation of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).--

On page 3, line 9, delete "micro-processor" and substitute --microprocessor--.

On page 6, line 1, delete "4,646,279" and substitute --4,646,270--.

On page 10, line 18, delete "Figure 7 shows" and substitute --Figures 7a and 7b show--.

On page 10, line 21, delete "Figure 8 shows" and substitute --Figures 8a and 8b show--.

On page 34, line 4, after "devices" insert --do--.

On page 41, line 1, delete "or' "and substitute -- or--.

On page 45, line 17, delete "Fig. 7" and substitute --Figures 7a and 7b--.

On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute -- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

151. A method of controlling a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises:

issuing a read request to the memory device, wherein in response to the read request, the memory device outputs first and second portions of data onto a bus;

sampling the first portion of data from the bus synchronously with respect to a rising edge transition of an external clock signal; and

sampling the second portion of data from the bus synchronously with respect to a falling edge transition of the external clock signal.

152. The method of claim 151 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device onto a bus in response to the read request; wherein

a first portion of the amount of data is sampled from the bus synchronously with respect to a rising edge transition of an external clock signal; and

a second portion of the amount of data is sampled from the bus synchronously with respect to a falling edge transition of the external clock signal.

153. The method of claim 152 wherein, in response to the read request, the first portion of the amount of data is output onto the bus after a delay time transpires.

154. The method of claim 153 further including providing access time information to the memory device.

155. The method of claim 154 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion of the amount of data is output onto the bus.

156. The method of claim 151 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

157. A controller device for controlling a synchronous memory device, the controller device comprising:

output driver circuitry to output a read request to the memory device, wherein in response to the read request, the memory device outputs a first and second portion of data onto a bus; and

input receiver circuitry to sample the first portion of data from the bus synchronously with respect to a rising edge transition of the external clock signal and a second portion of data from the bus synchronously with respect to a falling edge transition of the external clock signal.

158. The controller device of claim 157 wherein the input receiver circuitry includes first latch circuitry to latch the first portion of data, and second latch circuitry to latch the second portion of data.

159. The controller device of claim 157 further including a delay lock loop circuit coupled to the external clock signal, the

delay lock loop circuit generating a first internal clock signal, wherein the input receiver circuitry samples the first portion of data in response to the first internal clock signal.

160. The controller device of claim 159 wherein the delay lock loop circuit generates a second internal clock signal, wherein the input receiver circuitry samples the second portion of data in response to the second internal clock signal.

161. The controller device of claim 157 wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

162. The controller device of claim 157 wherein the input receiver circuitry samples an amount of data during a plurality of clock cycles of the external clock signal.

163. The controller device of claim 162 wherein the output driver circuitry provides information representative of the amount of data to output in response to a read request to the memory device.

164. The controller device of claim 163 wherein the read request and the information representative of the amount of data to output are included in a read request packet.

165. A method of operation of a memory controller device comprising:

issuing a write request to a memory device synchronously with respect to an external clock signal, wherein in response to the write request, the memory device inputs first and second portions of data;

outputting the first portion of data synchronously with respect to a first edge transition of an external clock signal; and

outputting the second portion of data from the bus synchronously with respect to a second edge transition of the external clock signal.

166. The method of claim 165 wherein the controller device outputs the first portion of data after a delay time transpires.

167. The method of claim 165 further including providing access time information to the memory device.

168. The method of claim 167 wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion of the amount of data is available on a bus.

169. The method of claim 165 wherein the first and second edge transitions of the external clock signal include voltage swings of less than one volt.

170. The method of claim 165 wherein the first portion of data and second portion of data include voltage swings of less than one volt.

171. The method of claim 165 wherein the data is output during a plurality of first and second edge transitions of the external clock signal.

172. The method of claim 165 further including providing block size information to the memory device, wherein the block size information is representative of an amount of data to be input in response to a write request.

173. The method of claim 172 further including outputting the amount of data which corresponds to the block size information.

174. The method of claim 173 wherein the data corresponding to the block size information is output during a plurality of first and second edge transitions of the external clock signal.

175. The method of claim 165 wherein the first edge transition of the external clock signal is a rising edge transition of the external clock signal, and the second edge transition of the external clock signal is a falling edge transition of the external clock signal.

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application Serial No. 09/510,213, which is a continuation of Application Serial No. 09/252,998, now U.S. Patent 6,032,214, which is a continuation of Application Serial No. 08/979,127, now U.S. Patent 5,915,105. Application Serial No. 09/510,213 is still pending.

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application 09/510,213, filed on February 22, 2000, which is a continuation of Application No. 09/252,998, filed on February 19, 1999 (now U.S. Patent 6,032,214), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No. 08/762,139, filed on December 9, 1996 (now U.S. Patent 5,809,263); which is a continuation of Application No. 08/607,780, filed February 27, 1996 (now abandoned); which is a continuation of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation or

related U.S. application data identified above. No new matter has been added.

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-175 to more fully protect the instant invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 2 and 10-13; page 14, lines 3-22, line 2; page 15, lines 18 to page 16, line 7; page 20, line 20 to page 21, line 20; page 23, line 6 to page 24, line 2; page 27, line 23 to page 28, line 20; page 46, line 19 to page 48, line 17; page 53, line 23 to page 59, line 2; and page 115, lines 10-22.

Applicants have also amended the specification to correct obvious spelling, typographical and grammatical errors. In addition, a new Abstract of the Disclosure is attached hereto. No new matter has been added.

Finally, accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. In that Request, Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in

particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Original Signed

Date: September 22, 2000

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ABSTRACT OF THE DISCLOSURE

A method of operation of a memory controller device, the method of operation comprises issuing a write request to a memory device synchronously with respect to an external clock signal, wherein in response to the write request, a memory device inputs first and second portions of data. The method of operation further includes outputting the first portion of data synchronously with respect to a first edge transition of an external clock signal; and outputting the second portion of data from the bus synchronously with respect to a second edge transition of the external clock signal. The first and second edge transitions of the external clock signal are of transitions of the same clock cycle.